C. Syllabus Detailing and Learning objectives

Module	Chapter	Detailed Content	Syllabus Detailing	Learning Objectives
Module 1	**CH 1 Intel 8086/8088 Architecture** (Hours -10)	8086/8088 Microprocessor Architecture, Pin Configuration, Programming Model, Memory Segmentation, Study of 8284 Clock Generator, Operating Modes, Study of 8288 Bus Controller, Timing diagrams for Read and Write operations, Interrupts.	**Purpose**: To make students understand the roll of microprocessor in computer based system and study basic software and hardware architecture of 16 bit 8086/8088 microprocessors and their comparison . Distinguish between microprocessor and microcontroller. Understand the different operating modes of 8086 processor. Discuss the concepts of memory segmentation and interrupts. **Scope –** **1. Academic Aspects-** Study of basic architecture and features of 16 bit microprocessor 8086/8088. **2. Technology Aspect- Understand the r**ole of microprocessor in microprocessor based system and how it is useful from basic operations to large calculations. **3. Application Aspect-** Differentiate between microprocessor and microcontroller. How the microprocessor used for general purpose applications and microcontroller for specific applications.	1. To Describe the features, software architecture (Programmer's model / Register set) and Hardware architecture (Block Diagram) of Intel 8086 / 8088 processor. **(R)** 2. To Distinguish between 8086 and 8088 processor. **(U**) 3. Use of memory segmentation with its pros and cons. **(A)** **4.** Describe the interrupt structure and how 8086 respond to interrupt **(U)**. 5. Draw the minimum mode CPU configuration and memory cycles **(R)**. 6. Draw the maximum mode CPU configuration for 8086 and the functions of Intel 8288 bus controller. **(R)**.

			Students Evaluation – 1. **Subjective questions** on 8086 architectures, pin configuration, Programming Model, Memory Segmentation 2. **Lab experiments**: Implement Five different experiments using assembly language for 8086 architecture. **3. Viva questions on architecture, pin configuration, difference between 8086 and 8088 etc.** **4. Class test based on modulle1 and 2.** **5. Lab test based on module 1.**	
Module 2	**CH 2** **8086 INSTRUCTION SET & PROGRAMMING** (Hours -08)	Instruction Set of 8086, Addressing Modes, Assembly Language Programming, Mixed Language Programming with C Language and Assembly Language.	**Purpose- T**his chapter focused on how do programming in Assembly language. Study of the different types of instruction set, assembler directives and addressing modes. Understand the different features and applications of ALP. How to use macro & procedure in programs. Differentiation between macros & procedure/function/subroutine. **Scope –** **1. Academic Aspects- To understand, how** to write program in assembly language for different applications. **2. Technology Aspect-** Understand the different features of ALP such as addressing modes, assembler directives, macros, procedures, arrays and string operations etc and Write macros as and when required to increase readability, productivity of program **3. Application Aspect-** Understand the basics and applications of ALP for Embedded system project development purpose.	1. Explain all the instructions with examples, formats and their use in the programming. **(U)** 2. Write assembly language program for 8086 using instruction set, assembler directives and addressing modes etc.**(R)** 3.Assess assembly language programs using TASM/MASM which are run on 8086 microprocessor system **(E)** 4.To Compare between Macros and procedure and Specify when to use macro and procedure. **(E)** 5. To define macros as and when required to increase readability, productivity of program. **(R)** 6. Experiment how to use C/C++ features in assembly language to make program for

			Students Evaluation – 1. Subjective questions on addressing modes and programming model. 2. Lab experiments: Implement Five different experiments using assembly language for 8086 architecture. **3. Viva questions on macros, procedures, assembler directives and instruction set etc.** **4. Class test based on modulle1 and 2.** **5. Lab test based on module 2.**	interactive and user friendly i.e . mixed mode programming **(AN)**
Module 3	**CH 3** - **System Designing With 8086** (Hours -12)	Memory Interfacing: SRAM, ROM and DRAM (using DRAM Controller Intel 8203). Applications of the Peripheral Controllers namely 8255PPI, 8253PIT, 8259PIC and 8237DMAC. Interfacing of the above Peripheral Controllers with 8086 microprocessor. Introduction to 8087 Math Coprocessor and 8089 I/O Processor.	**Purpose –**To provide the students with the knowledge of various memory and peripheral devices which are interfaced with microprocessors. Understand the features, applications, control word formats of Intel 8255, 8253, 8254, 8237 and how to interface these peripheral devices with 8086/8088 in minimum and maximum mode and how to make them programmable. **Scope –** **1. Academic Aspects-** Design microprocessor based system for the given specifications. **2. Technology Aspect-** **How to interface different peripheral devices and make them programmable for different applications. 3.** **Application Aspect-** **Use for real time applications such as square wave generation, traffic monitoring etc.**	1. Describe the working of 8259PIC. How to initialize and make 8259 Programmable to accept software and hardware interrupt requests in different operating modes.Also Illustrate the working of cascade mode. **(U)** 2. To Analyze the working of 8255 PPI. How it is used for 8 or 16-bit data transfer to /from peripheral devices and processor. **(AN**) 3. Illustrate the working of 8253 and show demonstration for different applications like Square wave generator, Interrupt on terminal, software trigger etc **(A**). 4. Explain the functionality of coprocessor and how it communicates with 8086 processor for execution of floating point operations. **(E)**

			Student Evaluation - 1.Multiple choice questions based on peripheral devices. 2. Subjective questions based on 8255,8253,8359,8257 , 8087, 8089 etc. 3. Group activity: Design of microprocessor based system for given specification. 2. Mini project: Based on real time applications.	5. Distinguish between minimum and maximum mode and Understand the concept of ODD and EVEN memory bank and how to interface SRAM and DRAM with 8086/8088 in minimum and maximum mode. **(U)** 6. Design microprocessor based system for given specification using minimum mode and maximum mode. **(C)**
Module 4	**CH 4** **Intel 80386dx Processor** (Hours -06)	Detailed study of Block diagram, Signal interface, Bus cycles, Programming model, Operating modes, Address translation mechanism in protected mode, Memory management, Protection mechanism.	**Purpose –**To introduce 32 bit architecture to the students. Understand the different advanced features of Intel 80386Dx processor over 8- bit architecture. Study of Software and hardware architecture of Intel 80386Dx. **Scope –** **1. Academic Aspects-** To learn the different advanced features of 32 bit architecture such as operating modes, memory management , paging , virtual memory , interrupts and multitasking. **2. Technology Aspect-** Understand the different operating modes and how to switch from real mode to protected mode. **3. Application Aspect-** To understand techniques for faster execution of instructions and improve speed of operation and performance of microprocessors.	1. List the advanced features of Intel 80386Dx processor such as ALU size, segmentation and paging , operating modes and protection mechanism etc. and compare the performance of 80386Dx with its predecessors **(R)** 2. Differentiate between Intel 80386Dx and 80386Sx w.r.t. address bus, data bus, cache memory , physical memory etc. **(AN)** 3.Describe software architecture (Programmer's model / Register set) and Hardware architecture (Block Diagram) of Intel 80386Dx processor **(U)**

			Student Evaluation - 1.Questions based on Finite Automata and lexical analyzer 2. Lab experiments based on hand written lexical analyzer 3. Mini project: NFA to DFA 4. GATE questions based on lexical analyzer .	4. Recall Logical, Linear and physical addresses and advantages and drawbacks of memory segmentation and paging mechanism.**(R)** 5. Compare different operating modes of Intel 80386Dx processor w.r.t. size of Physical Memory, segmentation and paging mechanism, enter and exit from operating modes etc.**(E)** 6. Give example what is need of protection mechanism in multitasking environment during segment and page level translation mechanism. **(U)**
Module 5	**CH 5 Pentium Processor** (Hours -08)	Block Diagram, Superscalar Operation, Integer & Floating Point Pipeline Stages, Branch Prediction, Cache Organization. Comparison of Pentium 2, Pentium 3 and Pentium 4 Processors. Comparative study of Multi core Processors i3, i5 and i7.	**Purpose –** At the completion of this module, students should be able to list the advanced features of Pentium processor. To understand the superscalar architecture, super pipelining and MESI protocol. Students able to differentiate between different Pentium family processors w.r..t. different parameters. **Scope –** **1. Academic Aspects-** Compare the advanced features of Pentium processor w.r.t. its predecessors. Differentiate between Von Neumann architecture, Hardwired architecture and Data flow architecture. **2. Technology Aspect-** **Understand and use the advanced features for large computations.** **3. Application Aspect-** Improve the speed of operations and performance of microprocessors.	1. List the advanced features of Pentium-1 such as DIB, superscalar architecture, Cache system , Branch prediction logic etc. and also relate P-1 with Intel 80386Dx, 80486Dx etc. **(R)** 2. Describe the superscalar architecture (More than one ALU) and super pipeline operations and analyze the performance of processor. **(U)** 3. Distinguish between different Pentium family processors w.r.t. different parameters. **(U)** 4. Describe the features of multicore processors like i3, i5 and i7.**(R)** 5. Predict how flushing / discarding of

			Student Evaluation – 1. Theory and viva questions on Integer and floating point pipeline stages, cache subsystem and Branch Prediction logic. 2. Lab experiment : Case study on Pentium family processors. 3. Assignment 3: Questions based on module 5.	instructions from large size queue problem is solve using Branch prediction logic.**(U)** 6. Recall cache subsystem and understand the concept of MESI protocol in code and data cache organization.**(R)**
Module 6	**CH 6 SuperSPARC Architecture** (Hours -04)	SuperSPARC Processor, Data Formats, Registers, Memory model. Study of SuperSPARC Architecture.	**Purpose –** Discuss the RISC The architecture of SPARC processor and its various data formats, registers, memory model of SPARC processor. The detailed study of Super SPARC and Ultra SPARC processor. **Scope –** **1. Academic Aspects-** **Identify and compare RISC and CISC processors.** **2. Technology Aspect-** Floating point units, cache organization, Integer pipelining and instruction grouping. **3. Application Aspect-** Distinguish between Sun micro system and Intel architecture. **Student Evaluation –** 1. Theory and viva questions on SuperSparc architecture, Data formats and circular window architecture. 2. Lab experiments based on Grouping the instructions. 3. Assignment 3: Module 3	1. List the different features of SUN SPARC such as 32 bit architecture, Superscalar architecture, pipeline etc.**(R)** 2. Distinguish between SuperSPARC and UltraSPARC processor w.r.t. Cache size, Instruction queue size etc.**(U)** 3. Explain Integer and floating point data formats of Sun SPARC processor. **(E)** 4. Draw the circular window structure of SuperSPARC processor.**(C)** 5. Describe the different instruction format and how to categorize the instructions into different data formats. **(U)** 6. Apply instruction grouping algorithm to group instruction into different groups to execute instructions parallel to improve the performance of Sun SPARC. (**A)**